

## ABSTRACT

A processor includes a first vector processing unit including a first register file and a first vector arithmetic logic unit; a second vector processing unit including a second register file and a second vector arithmetic logic unit wherein the first register file has a first plurality of cross connections to the second vector arithmetic logic unit; wherein the second register file ~~as a~~ <sup>has</sup> second plurality of cross connections to the first vector arithmetic logic unit.

6/16/04